MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
II B.Tech I Semester Supplementary Examinations, June/July 2024
Computer Organization
(CSE, CSE-CS, CSE-AIML, CSE-DS & B.Tech-AIML)

Roll No										

Time: 3 hours   **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	A	Differentiate multiprocessor and multicomputer.	[7M]
	B	Discuss multiplication algorithm with an example.	[7M]

OR

2		Describe the components of a computer arithmetic circuit and how a binary adder subtractor operates.	[14M]

SECTION-II

3		List and explain the basic micro-operations performed in computer architecture.	[14M]

OR

4		Define computer instruction. Discuss the instruction cycle and instruction codes.	[14M]

SECTION-III

5	A	Explain general register organization.	[7M]
	B	Explain RISC processor.	[7M]

OR

6		Discuss the components and characteristics of Micro Programmed Control Unit.	[14M]

SECTION-IV

7		Discuss memory hierarchy and explain RAM and ROM chips in detail.	[14M]

OR

8	A	Discuss the considerations and challenges involved in writing into a cache memory with an emphasis on the different mapping techniques.	[7M]
	B	Discuss auxiliary memory.	[7M]

SECTION-V

9	A	Explain the modes of transfer in Input-Output Organization, citing an example of Programmed I/O.	[7M]
	B	Discuss input – output sub systems.	[7M]

OR

10		Explain the basic concepts of pipelining and vector processing.	[14M]

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